CLAIMS:

1. A high-speed serial bit stream interface module comprising:

a line side interface that services a line side media, that receives a line side receive signal, and that transmits a line side transmit signal;

a board side interface that services a plurality of transmit bit streams and a plurality of receive bit streams;

at least one multiplexer that multiplexes the plurality of transmit bit streams to produce the line side transmit signal;

at least one demultiplexer that demultiplexes the line side receive signal to produce the plurality of receive bit streams; and

a plurality of signal conditioning circuits, each of which services a respective bit stream of the plurality of transmit bit streams and the plurality of receive bit streams.

2. The high-speed serial bit stream interface module of claim 1, wherein each of the plurality of signal conditioning circuits spectrally shapes its serviced bit stream.

3. The high-speed serial bit stream interface module of claim 2, wherein the plurality of signal conditioning circuits spectrally shape their respective bit streams to remove deterministic jitter.

4. The high-speed serial bit stream interface module of claim 2, wherein the plurality of signal conditioning circuits spectrally shape their respective bit streams to remove inter symbol interference.

5. The high-speed serial bit stream interface of claim 1, wherein each of the plurality of signal conditioning circuits comprises:

a limiting amplifier that receives a serviced signal and that amplifies the serviced signal to produce the serviced signal in a desired output range;

a clock and data recovery circuit having an adjustable Phase Locked Loop (PLL) bandwidth that communicatively couples to the output of the limiting amplifier and that receives, recovers, and reclocks the serviced signal; and

wherein the PLL bandwidth of the clock and data recovery circuit is controllable to correspond to the signal characteristics of the serviced signal.

6. The high-speed serial bit stream interface of claim 5, wherein:

the PLL bandwidth of signal conditioning circuits servicing transmit signals is based upon output characteristics of a device producing the transmit signals to the board side interface; and

the PLL bandwidth of signal conditioning circuits servicing receive signals is based upon output characteristics of a device producing the receive signals to the line side interface.

7. The high-speed serial bit stream interface of claim 5, wherein the signal conditioning circuits each further comprise:

an output pre-emphasis circuit communicatively coupled to the output of the clock and data recovery circuit that controllably modifies the spectrum of the serviced signal to pre-compensate for spectral characteristics of a signal path upon which the serviced signal will be output.

8. The high-speed serial bit stream interface of claim 5, wherein the signal conditioning circuits each further comprise:

an equalizer communicatively coupled to the output of the limiting amplifier that controllably spectrally shapes the serviced signal to compensate for spectral characteristics of a signal path from which the serviced signal was received.

9. The high-speed serial bit stream interface of claim 5, wherein the signal conditioning circuits each further comprise:

a limiting amplifier that receives the serviced signal and that controllably amplifies the serviced signal to produce the serviced signal in a desired output range.

10. The high-speed serial bit stream interface of claim 1, further comprising:

a receive lane synchronizer that services the plurality of receive bit streams; and

a transmit lane synchronizer that services the plurality of transmit bit streams.

11. The high-speed serial bit stream interface of claim 11, wherein:

the receive lane synchronizer operates by inserting at least one bit pattern into the plurality of receive bit streams; and

the transmit lane synchronizer operates by inspecting at least one bit pattern contained in the plurality of transmit bit streams and realigning the plurality of transmit bit streams when required as determined by the inspection.

12. The high-speed serial bit stream interface of claim 1, further comprising:

a receive Forward Error Correction (FEC) block that services the plurality of receive bit streams; and

a transmit FEC block that services the plurality of transmit bit streams.

13. A high-speed serial bit stream interface module comprising:

a back plane/box interface that services a first plurality of transmit bit streams and a first plurality of receive bit streams;

a board side interface that services a second plurality of transmit bit streams and a second plurality of receive bit streams;

at least one demultiplexer that demultiplexes the first plurality of receive bit streams to produce the second plurality of receive bit streams;

at least one multiplexer that multiplexes the second plurality of transmit bit streams to produce the first plurality of transmit bit streams; and

a plurality of signal conditioning circuits, each of which services a respective bit stream of the first plurality of transmit bit streams and the first plurality of receive bit streams.

14. The high-speed serial bit stream interface module of claim 13, wherein each of the plurality of signal conditioning circuits spectrally shapes its serviced bit stream.

15. The high-speed serial bit stream interface module of claim 14, wherein the plurality of signal conditioning circuits spectrally shape their respective bit streams to remove deterministic jitter.

16. The high-speed serial bit stream interface module of claim 14, wherein the plurality of signal conditioning circuits spectrally shape their respective bit streams to remove inter symbol interference.

17. The high-speed serial bit stream interface of claim 13, wherein each of the plurality of signal conditioning circuits comprises:

a limiting amplifier that receives a serviced signal and that amplifies the serviced signal to produce the serviced signal in a desired output range;

a clock and data recovery circuit having an adjustable Phase Locked Loop (PLL) bandwidth that communicatively couples to the output of the limiting amplifier and that receives, recovers, and reclocks the serviced signal; and

wherein the PLL bandwidth of the clock and data recovery circuit is controllable to correspond to the signal characteristics of the serviced signal.

18. The high-speed serial bit stream interface of claim 17, wherein:

the PLL bandwidth of signal conditioning circuits servicing transmit signals is based upon output characteristics of a device producing the transmit signals to the board side interface; and

the PLL bandwidth of signal conditioning circuits servicing receive signals is based upon output characteristics of a device producing the receive signals to the line side interface.

19. The high-speed serial bit stream interface of claim 17, wherein the signal conditioning circuits each further comprise:

an output pre-emphasis circuit communicatively coupled to the output of the clock and data recovery circuit that controllably modifies the spectrum of the serviced signal to pre-compensate for spectral characteristics of a signal path upon which the serviced signal will be output.

20. The high-speed serial bit stream interface of claim 17, wherein the signal conditioning circuits each further comprise:

an equalizer communicatively coupled to the output of the limiting amplifier that controllably spectrally shapes the serviced signal to compensate for spectral characteristics of a signal path from which the serviced signal was received.

21. The high-speed serial bit stream interface of claim 17, wherein the signal conditioning circuits each further comprise:

a limiting amplifier that receives the serviced signal and that controllably amplifies the serviced signal to produce the serviced signal in a desired output range.

22. The high-speed serial bit stream interface of claim 13, further comprising:

a receive lane synchronizer that services the first plurality of receive bit streams; and

a transmit lane synchronizer that services the first plurality of transmit bit streams.

23. The high-speed serial bit stream interface of claim 22, wherein:

the receive lane synchronizer operates by inserting at least one bit pattern into the first plurality of transmit bit streams; and

the transmit lane synchronizer operates by inspecting at least one bit pattern contained in the first plurality of transmit bit streams and realigning the first plurality of transmit bit streams when required as determined by the inspection.

24. The high-speed serial bit stream interface of claim 14, further comprising:

a receive Forward Error Correction (FEC) block that services the first plurality of receive bit streams; and

a transmit FEC block that services the first plurality of transmit bit streams.